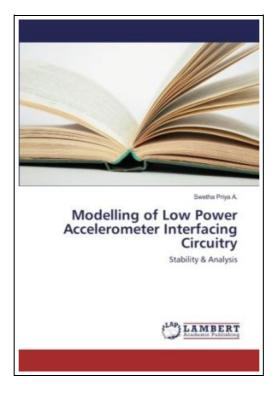
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MODELLING OF LOW POWER ACCELEROMETER INTERFACING CIRCUITRY



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LAP Lambert Academic Publishing Feb 2017, 2017. Taschenbuch. Condition: Neu. Neuware - The surge for silicon accelerometers with low form factor-g and low noise-power-voltage interfacing readout systems are of paramount interest for the next generation's light-weight, low-cost Inertial Measurement Units (IMU's) and microgravity measurement systems, opening the scope for a wide range of low-power applications in VLSI-MEMS technology. This key-informative book gives a head start for reader to participate in emerging fields of application. It deals with the designing, modelling, simulating & analyzing the low power- low noise - high performance generic interfacing system that utilizes switched capacitive technique to read out electro-mechanical accelerometer values within the range of ±2g. The mixed-signal topology is developed to be highly programmable using MATLAB/SIMULINK environment to analyze the noise contributors and system-level circuit non-idealities to make the model a reliable tool in identifying the performance limits of the mixed-signal embedded high speed circuitry to ensure power & noise reduction. This book is for all enthusiastic readers & innovators guiding them to build more realistic & reliable systems for VLSI World. 196 pp. Englisch.

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