Gate Stack and Silicide Issues in Silicon Processing: Volume 611 (Paperback)

By -

CAMBRIDGE UNIVERSITY PRESS, United Kingdom, 2014. Paperback. Condition: New. Language: English . Brand New Book ***** Print on Demand *****. As the feature size of microelectronic devices approaches the deep submicron regime, the process development and integration issues related to gate stack and silicide processing are key challenges. Gate leakage is rising due to direct tunneling. Power and reliability concerns are expected to limit the ultimate scaling of SiO2-based insulators to about 1.5nm. Gate insulators must not deleteriously affect the interface quality, thermal stability, charge trapping, or process integration. Metal gate materials and damascene gates are being investigated, in conjunction with the application of a high-permittivity gate insulator, to provide sufficient device performance at ULSI dimensions. The silicidation process is also coming under pressure. Narrow device widths and decreasing junction depths are making the formation of low-leakage, low-resistance silicide straps extremely difficult. Producing shallower junctions via ion implantation is inhibited by transient enhanced diffusion and low beam currents at low implantation energies. Gate stack and contact film effects, such as point defect injection, extended defect formation, and stress on ultrashallow junction formation must be considered.

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